Hardware Accelerated Algorithms for 2nd Level Trigger of Very Forward Detectors at LHC

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Abstract

Data acquisition systems in High Energy Physics need to cope with increasing requirement of transmission bandwidth and storage capability. The LHC increase of luminosity and the bunch space reduction, after the first machine shutdown period, will produce more interactions per bunch crossing and increase the level of signal background.

We present the design and study of second level trigger algorithms implemented in the data acquisition system of the TOTEM Experiment [1]. The project aims to increase the efficiency of the actual readout system by filtering on-line data, preserving the physics information of interest and better exploiting the available storage bandwidth.

Hardware Platform and System Architecture

The SRS (Scalable Readout System) [2] designed and developed by the RD51 community has been chosen as the hardware platform for the upgrade of the TOTEM DAQ System and to host the 2nd level trigger hardware algorithm. The SRS offers enough computing resources having FPGA Virtex devices from Xilinx on board of both the FEC and the SRU modules.

The system architecture has been designed following the block scheme shown in the picture. All interfaces between blocks are standard AXI-stream data streams. Data are first received as serial streams (Fb/1b coding) then parallelized and checked for CRC errors. In the following stage the Synch/Checker block inspects the frames and checks the VRF chip Bunch Counter and Event Counter alignment. The Cluster Finder block takes care of finding clusters. The starting strip and the size information are used to describe a cluster. Once clusters are built the Pattern Finder block runs the tracking algorithm and sends the track data to the Event Builder block for the final subevent formatting.

System Design and Test Work-flow

The project takes advantage of modern design techniques in both design synthesis and verification adopting SystemVerilog language and Universal Verification Methodology (UVM) [3]. Full device simulation, including the algorithm core along with all connected interfaces and modules was developed in the described environment.

The System Verilog DPI (Direct Programming Interface) enables calling C/C++ library routines directly in the simulation environment. This allows to integrate in a common simulation environment firmware blocks and software components already used by the Experiment, such as software classes for raw data extraction and for data generation. A novel test vector generation facility has been designed to inject into the design test patterns extracted from real data produced by the TOTEM experiment in the past data taking campaigns, or simulated data generated by Monte Carlo simulations of the Experiment.

References

[1] G. Anelli et al., The TOTEM Experiment at the CERN Large Hadron Collider, 2008 JINST 3 S08007

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