TOTEM	TOTEM Experiment TOTEM ELECTRONICS SPECIFICATION		
TOTEM Project Document No: **TOTEM GEMEL SPEC**	*Institute Document No.* EDMS id	*Created:* **27/01/06** *Modified:*	 *Rev. No.:* **0.0**

TOTEM GEM (T2) ELECTRONICS SPECIFICATION

Abstract

This document provides the full specification of the GEM Electronics of the TOTEM experiment. It is meant as a working document during the development, fabrication and final commissioning of the electronics in the experiment. This document is a complement to the TOTEM general electronics specification: the electronics for the three TOTEM subdetectors have many parts in common. This document details the specifics for the GEM detector. It has been prepared with the help from the people working on the GEM electronics at CERN and in Pisa/Siena.

Prepared by:	*Checked by:*	*Approved by:*
W. Snoeys PH-MIC	**Pierre Jarron PH-MIC** **Mike Letheren PH-MIC** **Ernst Radermacher PH-TOT** **Karsten Eggert PH-TOT**	**W. Snoeys PH-MIC**

Distribution List

Checking committee

Table of Contents

1 Introduction

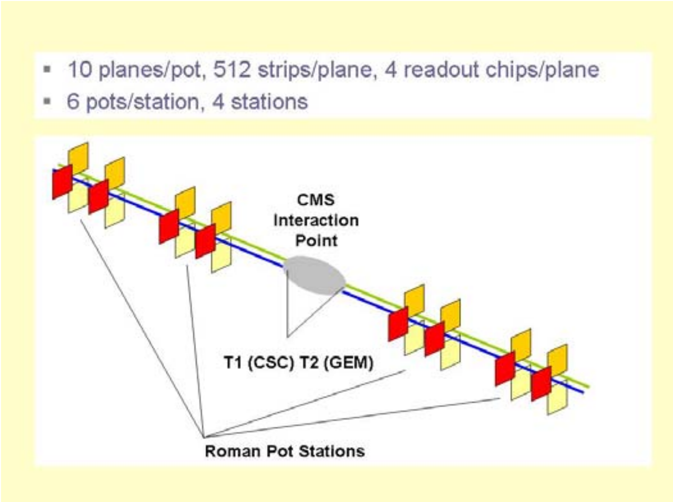

Fig. 1. The full TOTEM detector with 3 subdetectors.

The GEM detector is one of the two gas detectors placed in the CMS cavern (see fig.1). The GEM detector consists of four sectors, two on each side of the interaction point, and each containing 10 GEM half planes (see fig.2). Each half plane covers an angle around the beam pipe of slightly over 180 degrees. The detector contains 65 pie-shaped sectors which each consist of 24 pads in the radial direction. 13 VFATs per half plane are used to read out 5 adjacent pie-shaped sectors, and to provide the trigger bits corresponding to these 5 sectors. The readout of 5 times 24 or 120 pads leaves 8 out of 128 inputs unused in the VFATs used for the pads in the GEMs. In addition there are 256 strips in the ϕ direction which are interrupted very close to the axis of symmetry resulting in 512 strips which will be read out also by 4 VFAT chips, so there are 17 VFATs per detector (half)plane.

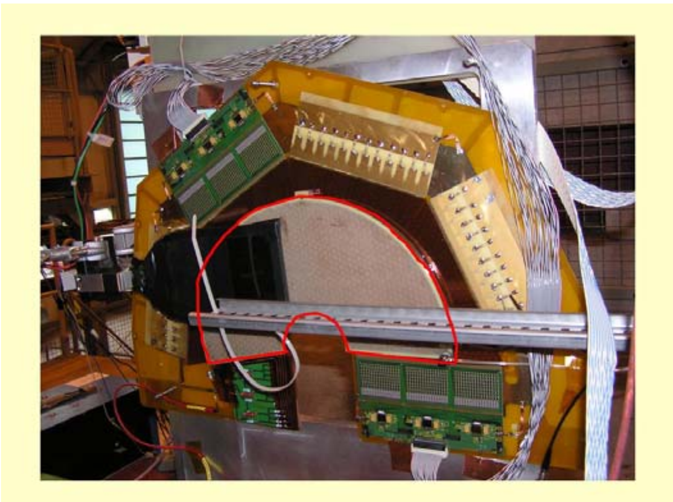

Fig. 2. 2004 version of a GEM detector half plane. The read figure indicates the surface occupied by the detector itself. The surrounding electronics will have to be replaced by a more compact version which includes VFAT chips.

I. Occupancy and its impact on the readout architecture and data rate

The choice of 10 planes per GEM sector offsets any detection inefficiencies and allows to effectively eliminate background by requiring co-linear hits in a certain number of the detector planes. The pad occupancy is forecast to be about 1.2 %. On the strips the number is much higher (up to 20 % or so). To deal with the larger occupancies and to standardize across detectors it was decided to use non-zerosuppressed serial readout (1 bit/channel). Normally the data from 16x8 = 128 VFATs (so 8 GOL links fully equipped with VFATs) will fill up the full capacity of one FRL. We have 170x2 VFATs per side for the GEM, so we need 6 FRLs for the GEM readout. The event size per FRL is 2kByte, and the maximum nominal level 1 trigger rate is 100 kHz, resulting in a maximum data rate for the GEM of 6x2kBytex100kHz=1.2 GByte/sec. 170 VFAT require 11 GOL optical links between detector and counting room to transmit the data, so we have 22 GOL optical links per side for the GEM detector.

II. Trigger data, coincidence and latency

Apart from the binary data which is stored in a digital memory and read out upon the application of a readout trigger, the VFAT also provides eight trigger bits which can be configured to correspond to a certain grouping of front end channels. For the GEM all 8 VFAT trigger outputs are used which each correspond to a group of 15 GEM pads in groups of 5 in the ϕ direction by 3 in the radial direction. This trigger data results in 104 trigger bits per GEM half plane. These bits are put into coincidence for 10 halfplanes by means of the coincidence chip (CC chip), which can be configured to match exactly the GEM geometry. The CC chip will require x bits out of 10 at the same coordinate in r and e ϕ, where x is programmable. An event during which the detector stack within the pot was hit by a shower of particles can be rejected by means of a programmable multiplicity cut implemented in the CC chip. After this first level coincidence the number of trigger bits sent to the counting room is 104 trigger bits for 10 half planes or 416 for the entire T2 detector.

2 The electronics or horseshoe card on the GEM detector plane

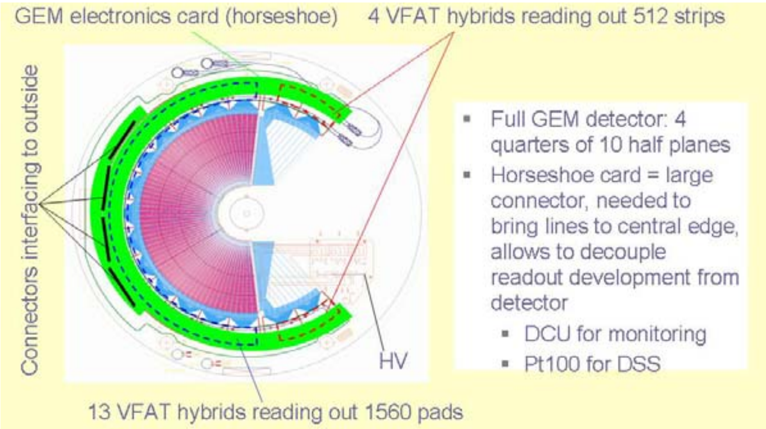

Fig. 3. TOTEM GEM detector half plane is read out by 17 VFAT chips. The VFAT chips are mounted on VFAT hybrids (see fig. 4) which are connected to the detector by a connector and to the outside world by means of the GEM horseshoe shaped electronics card.

Fig. 3 shows a drawing of a TOTEM GEM detector half plane. The detector's sensitive surface is denoted in pink. The GEM electrodes collecting the charge are read out by 17 VFAT hybrids (see Fig. 4), of which 4 are reading the 512 strips, and 13 the 1560 pads. The VFAT hybrids are connected by means of a small cable to the GEM electronics card (horseshoe shaped) which acts as a large connector between the hybrids and the 4 80 pin connectors to which cables are connected leading to the outside world. The horseshoe shaped card contains in addition one or two DCU chips needed for monitoring of voltages and temperature, and some PT100 thermistors. Some of these thermistors are read out using the DCUs, but one of them is provided for the detector safety system and will be linked directly to this system at least for a few detector planes.

3 The GEM VFAT hybrid

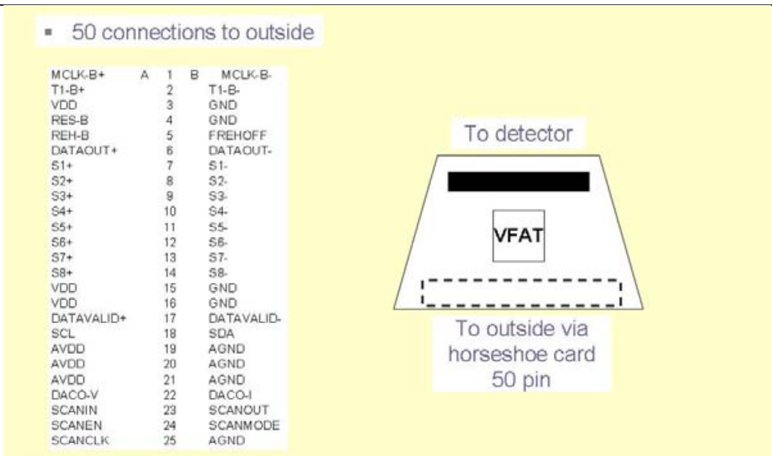

Fig. 4. The TOTEM hybrid with its connections to the horseshoe card. The hybrid is connected to the GEM detector by a 130 pin connector, and to the outside world using a 50 pin connector.

Fig. 4 shows a drawing of a TOTEM VFAT hybrid with its connections to the horseshoe card. The hybrid is connected to the GEM detector by 130 pin connector, which has facilitated the testing of the detectors: special test cards could now be plugged in and out for these tests. Previously one needed to wire bond for these tests.

The 50 pin connector links the hybrid to the horseshoe card by means of a small cable. This has allowed to decouple the development of the electronics from that of the detector. The connection list clearly shows the 8 trigger outputs from the VFAT.

4 VFAT protection for gas detectors

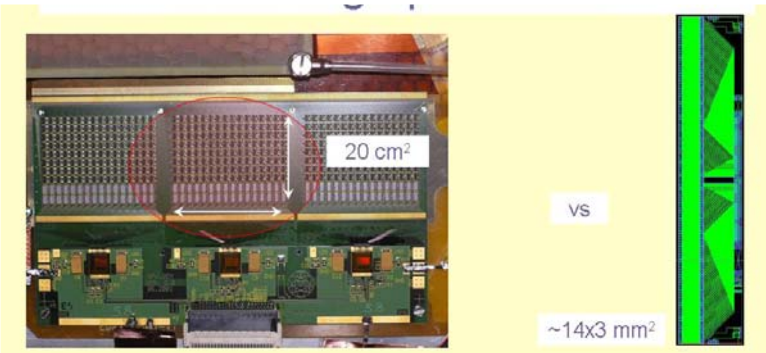

Fig. 5. To reduce the cost and the space occupied by a discrete protection (left) of the readout against discharges in the chamber, TOTEM developed an integrated protection circuit taking about 50 times less space.

Gas detectors can present discharges which deposit large amounts of charge on the readout electrodes. Without special precautions this can easily lead to destruction of the front end chips. Fig. 5 shows the discrete protection structure used in the COMPASS experiment, which takes about 20 square cm in area, prohibitive for the TOTEM GEM which has to be inserted in a very confined space. Therefore a new integrated protection circuit was developed. Figure 5 illustrates that this integrated protection circuit takes 50 times less area. The integrated protection structure consists of a series resistor, two reverse biased diodes, and an AC coupling.

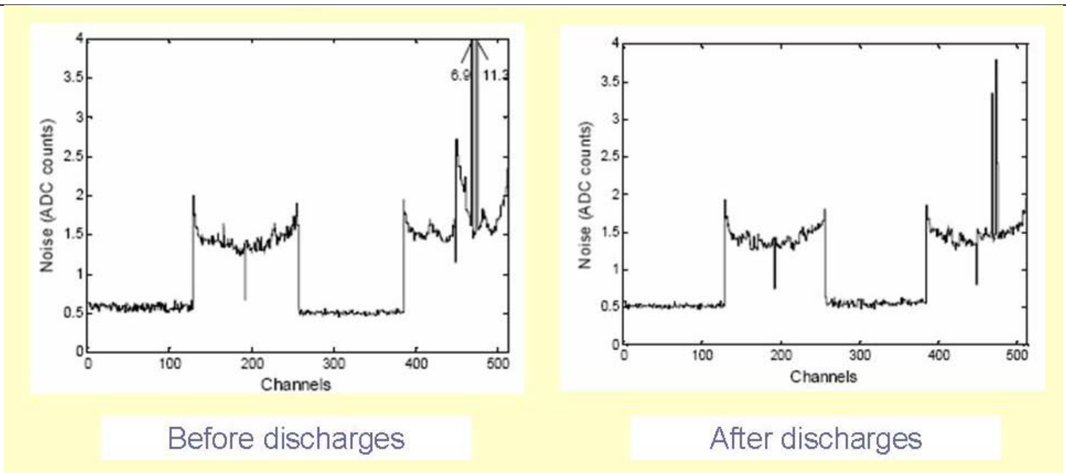

Fig. 6. Comparison of electronics performance before and after exposure to discharges induced in the GEM chamber. No significant deterioration was observed, so the protection circuit correctly performs its function.

This integrated protection structure was tested (see fig. 6), and after many hundreds of induced discharges in the GEM chamber no visible deterioration of the readout electronics (tested with APV chips) could observed. Without the protection the APV chips would not have survived. This protection circuit will be integrated into the VFAT version for the gas detectors, but with omission of the AC coupling which is not required for the VFAT. For the silicon in the Roman Pots a version of the VFAT will exist without this protection which is not needed in that case.

5 GEM electronics system overview

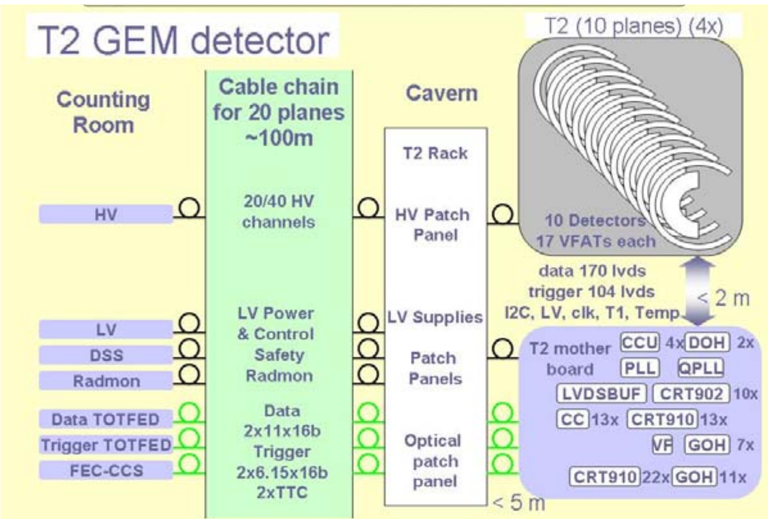

Fig. 7. Overview of the GEM electronics system

Fig. 7 gives an overview of the GEM electronics system. The basic unit is a quarter of the total GEM detector consisting of 10 half planes each equipped with 17 VFAT hybrids and the GEM horseshoe card. The half planes are fed directly with their HV supply, but all the other electrical connections to the outside pass via the T2 GEM mother board, which is in close proximity of the detector (underneath, but just outside the shielding). This board (see the next section) contains the TTC, the trigger and the data system for the detector and provides additional connections for power, safety and radiation monitoring. From this board optical fibers leave to the optical patch panel in the T2 rack (which serves one side of the GEM detector or two quarters). This rack contains the power supplies, and patch panels for LV, HV, safety and radiation monitoring. From this rack cables – electrical and optical leave to link the detector to the counting room via the 100 m long cable chain.

The electronics was standardized across the three different TOTEM subdetectors : the data is received by the TOTEM FED equipped with the optoRX mezzanine, the trigger signals as well, and the TTC system is based on the CMS ECAL and Tracker control loop with FEC-CCS and CCU token ring. This is described in detail in the general TOTEM electronics specification and is not further discussed here.

6 GEM motherboard

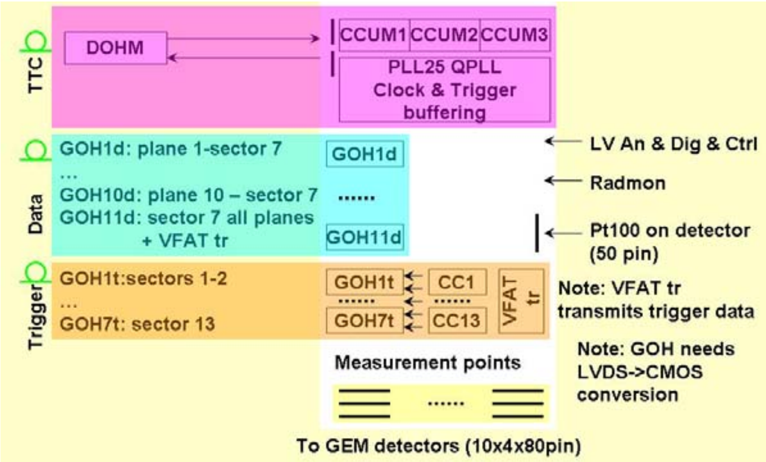

Fig. 8. Overview of the GEM mother board, containing TTC, data and trigger functions and connections for LV, radiation monitoring and temperature monitoring (for DSS).

The GEM motherboard serves one quarter of the full GEM detector and has the following functions:

a. The full TTC functionality for the TTC of the 10 half planes: the DOHM functionality, i.e. the two Digital Opto-Hybrids (DOH) converting the optical signals from and to electrical signals for the slow control, and the local electrical token loop (CCU-ring) including all the CCU modules for the 10 half planes. The CCU module used is the CCUM-tib-tec.

b. The trigger generation: it contains 13 CC chips carrying out the coincidence of the 10 x 13 x 8 VFAT trigger signals from the detector pads which reduces the total number of trigger bits per quarter by a factor 10 to 104 bits. These bits are transformed from LVDS into CMOS and then fed into 7 GOH optohybrids for transmission to the counting room. In addition these bits are presented to an on-board VFAT which records these trigger bits and inserts upon receipt of L1 into the data stream.

c. The data path: the 10 x 17 VFATs on the detector quarter feed their data after LVDS to CMOS conversion into 11 GOH optohybrids for transmission to the counting room.

d. The electrical signals from and to the detector are implemented by 40 80-pin connectors. Measurement points are provided to ease debugging and verification.

e. The GEM card receives the LV from the supplies and powers the detector. It also provides connections to and from the detector for radiation monitoring and detector safety (temperature)

By placing all optohybrids on the GEM Motherboard allows TTC, data and trigger paths for one quarter of the detector to be implemented using 7+11+8 = 26 optical fibers.

7 Test cards

To be able to test produced detectors even prior to the availability of the final electronics several printed circuit boards have been designed and fabricated:

1. Cards linking GEM detector electrodes to ground using resistors (one for the strips, and one for the pads).
2. An APV hybrid

3. An adapter card to test the detector using the APV hybrid in combination with the ARCs system.

The latter two cards have just returned from fabrication and are currently under test.

8 References

1. TOTEM TDR
2. Addendum to the TOTEM TDR
3. TOTEM general electronics specification
4. P. Aspell: VFAT digital part specification
5. J. Kaplon: Analog Front End
6. P. Chalmet, W. Snoeys: Coincidence Chip specification
7. P. Chalmet, W. Snoeys: LVDS repeater chip specification