

TOTEM**TOTEM Experiment****TOTEM ELECTRONICS SPECIFICATION***TOTEM Project Document No:***TOTEM RP EL SPEC***Institute Document No.*

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Created: **02/02/06***Modified:**Page:* **1 of 8***Rev. No.:* **0.0****TOTEM ROMAN POT ELECTRONICS SPECIFICATION***Abstract*

This document provides the full specification of the Roman Pot Electronics of the TOTEM experiment. It is meant as a working document during the development, fabrication and final commissioning of the electronics in the experiment. This document is a complement to the TOTEM general electronics specification: the electronics for the three TOTEM subdetectors have many parts in common. This document details the specifics for the Roman Pot detector. It has been prepared with the help from the people working on the Roman Pot electronics at CERN.

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1 Introduction

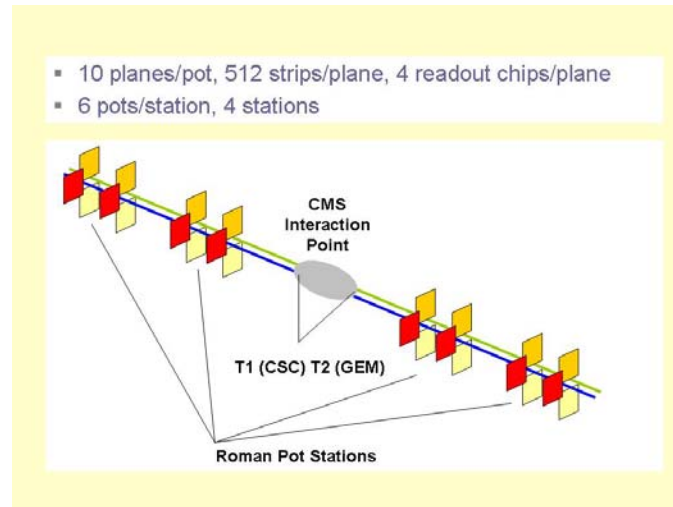


Fig. 1. The full TOTEM detector with 3 subdetectors.

The full TOTEM detector (Fig.1) (Ref. 1 TDR) consists of the Roman Pots housing silicon strips for tracking and triggering purposes, the T1 detector with Cathode Strip Chambers, and the T2 detector. The T1 and T2 detectors are located on each side of the CMS interaction point in the very forward region, but still within the CMS cavern. Two Roman Pot stations are foreseen on each side of the interaction point at 220 m and 150 m with the possibility to add a third station at 80 m. Each Roman Pot station consists of two groups of three Roman Pots at a distance of a few meters to obtain a sufficiently large lever arm to establish co-linearity with the LHC beam for the tracks prior to generating a level one trigger for the corresponding event. Three Roman Pots were foreseen in one group to approach the beam with detector stacks from three different sides (top, bottom and one side, the other side is impossible due to the presence of the second beam pipe).

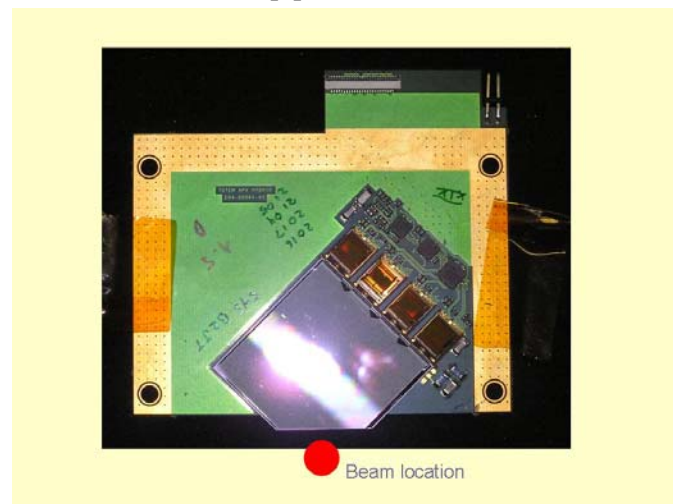


Fig. 2. 2004 version of a detector hybrid for the Roman Pot, equipped with the TOTEM silicon detector, and four readout chips each reading out 128 strips. The red dot in the figure indicates the location of the beam (passing the detector perpendicularly). The detector edge near the beam has been optimized for minimum dead space.

Each Roman Pot contains a detector package of 10 hybrids each equipped with a silicon strip detector with 512 strips read out by 4 VFAT chips each containing 128 electronic channels. Fig. 2 shows a picture of the 2004 version of the hybrid containing 4 APV chips. The detector strips are oriented at an angle of 45 degrees (from bottom left to top right in the picture) and the detector hybrids in the detector stack are mounted face to face in

which case their strips are at a 90 degree angle with respect to each other providing two coordinates (“U” and “V”). The detector has been carefully designed to have the minimum amount of dead area on its side nearest to the beam.

I. Occupancy and its impact on the readout architecture and data rate

The choice of 10 planes per pot offsets any detection inefficiencies and allows to considerably eliminate background by requiring collinear hits in a certain number of the detector planes (see TDR and work by Mario). The worst case average strip occupancy forecast by calculations and simulations is 4 %. The uncertainty on this value, the marginal benefit for this value, the higher occupancies in other TOTEM detectors, and the push for standardization across subdetectors made us discard zero-suppression on the VFAT binary data (1 bit/channel). The VFAT (see the separate document for its detailed specifications) therefore provides serial data where the position of the data within the data stream corresponds to the physical location of the channel on the readout chip (and hence on the strip detector). The data itself corresponds to 128 bits/chip, or at the maximum level 1 trigger rate of 100 kHz to 12.8Mbit/sec/chip or 1.6MByte/sec/chip. There are 40 VFATs per Roman Pot (4x10 planes) plus one placed on the motherboard to read out the trigger bits. This results in three GOHs per pot (of which one is only filled up at 9/16 of its capacity), which allows to combine the data from three Roman Pots (123 chips) into one FRL (max average rate of 200 MByte/sec). One Roman Pot station consists of 6 pots, and outputs 18 data fibers. Therefore 8 FRL's will be needed for the 4 Roman Pot stations foreseen.

II. Trigger data, coincidence and latency

Apart from the binary data which is stored in a digital memory and read out upon the application of a readout trigger, the VFAT also provides eight trigger bits which can be configured to correspond to a certain grouping of front end channels. For the Roman Pots only 4 trigger outputs per VFAT are used which each correspond to a group of 32 adjacent strips. This trigger data results in 16 trigger bits per plane which have to be put into coincidence first with the trigger bits from the other planes within one pot, and then with the coincidence result generated in the corresponding pot at a few meters distance. The coincidence within the pot has to establish whether at least x out of 5 detectors in U and x out of 5 in V were hit. An event where the detector stack within the pot was hit by a shower of particles should be rejected by means of a multiplicity cut. The further coincidence between the two corresponding pots (e.g. the two horizontal pots) should establish co-linearity with the primary beam where the maximum angle should be programmable up to a distance of 5 trigger sectors between the tracks in two corresponding pots.

For the Pots at 220 m a more detailed study has been carried out on the cable length between the pots and the global trigger box in the counting room which has been minimized to about 260 m. Taking into account the travel time of the particles from the interaction point where the event took place to the Roman Pots ($=220 \text{ m} \cdot 3.3 \text{ ns/m}$) and the cable delay ($=260 \text{ m} \cdot 5 \text{ ns/m}$) yields an evaluation time of

$$85 \cdot 25 \text{ ns} - 220 \cdot 3.3 - 260 \cdot 5 = 2125 - 726 - 1300 = 99 \text{ ns} < 4 \text{ BC} !$$

or less than 4 (!) 25ns bunch crossings for the evaluation of the coincidence. Therefore optical transmission using data serialization with its inherent latency (5 ns/m) has been discarded in favour of parallel electrical transmission over a fast cable ($\sim 4.2 \text{ ns/m}$) of the 32 coincidence bits generated per Roman Pot. If one assumes 270 m to include some margin, one obtains:

$$85 \cdot 25 \text{ ns} - 220 \cdot 3.3 - 270 \cdot 4.2 = 2125 - 726 - 1124 = 265 \text{ ns} \sim 10 \text{ BC}$$

So, this gives very little but at least some margin to generate the trigger within the required latency of 85 bunchcrossings.

This relatively large number of bits has been retained to include some coordinate information already in the trigger. While currently an FPGA is still a possibility for the trigger box in the counting room, it has been decided to use a full-custom programmable coincidence chip CC for the (very simple) local coincidence. This full-custom chip programmable using the slow-control system provides a one clock-cycle latency and full radiation hardness. The details of this chip are described in a separate document (see references). Normally two such chips will be used per Roman Pot. The trigger bits in the counting room will be put into coincidence or anticoincidence for Roman Pot stations on opposite sides of the interaction point to trigger on or reject elastic events. In total there will be 32 times 24 or 768 trigger bits sent to the counting room by the Roman Pots.

III. Trigger data transmission hardware

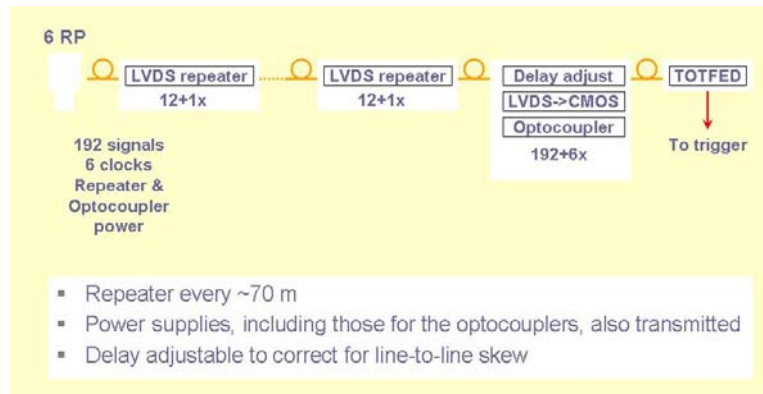


Fig. 3. Principle of trigger data transmission with several stages of repeaters.

Choosing electrical transmission of the trigger bits over such long distance requires care to preserve signal integrity. This can only be achieved by restoring the LVDS signals to full levels at regular intervals over the transmission distance. A special integrated circuit was designed for this purpose: the LVDS repeater chip can treat 16 LVDS channels in parallel and was designed in special layout to guarantee radiation tolerance. It will be submitted together with the VFAT. More detailed documentation can be found in the LVDS repeater chip specification. Fig. 3 shows the principle to transmit the trigger bits: at regular intervals of about 70 m a repeater station is introduced which consists of 13 repeater chips with cable connectors. Power for the repeaters is supplied along the cable as well, and filtered on board. In the counting room optocouplers are used to isolate the signals from the counting room. The optocouplers have to be powered from the detector side. Some way to delay the signal per channel is foreseen to equalize overall delay (can be using switches or jumpers to bypass a long signal path or not). After LVDS to CMOS conversion, the bits can be fed into a TOTFED for further processing and final coincidence.

2 The silicon detector hybrid

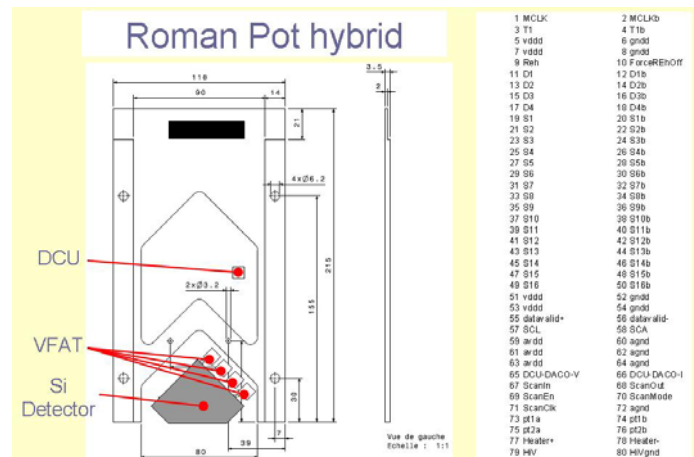


Fig. 4. The new Roman Pot detector hybrid will contain 4 VFATs linked to a detector with 512 strips. A DCU chip is mounted for monitoring. The connection to the motherboard and the outside world is realized by a 80 pin connector.

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The silicon detector hybrid (Figure 4) carries detector and 4 VFAT readout chips and a DCU chip. The hybrid is interfaced to the outside world by means of an 80 pin connector linked to a flat cable. The VFAT is biased internally now making the new VFAT hybrid much less complex. Each VFAT will send 4 trigger outputs to the motherboard for further coincidence, resulting in 16 trigger outputs per hybrid (so 32 wires for LVDS occupying 40 % of the 80 pin connector). The 80 pin connector linking the hybrid to the motherboard carries also HV and LV power, clock and trigger signal, and also connections for a heater and a pt100 thermistor for temperature control.

The strips on the detector are at 45 degrees angle with respect to the edge close to the beam (see Fig. 2). Flipping the detector hybrid and mounting it face to face with the next one results in orthogonal strips giving the U and V coordinate information. To avoid losing space all electrical components are foreseen on one side (the right looking from the top) so that these do not overlap for the two cards mounted face to face.

Each Roman Pot contains 10 detector hybrids mounted face to face in pairs. All 10 hybrids are connected to the Roman Pot motherboard via a cable connecting to the 80 pin connector. This cable is the only link to the outside world.

3 Roman Pot motherboard

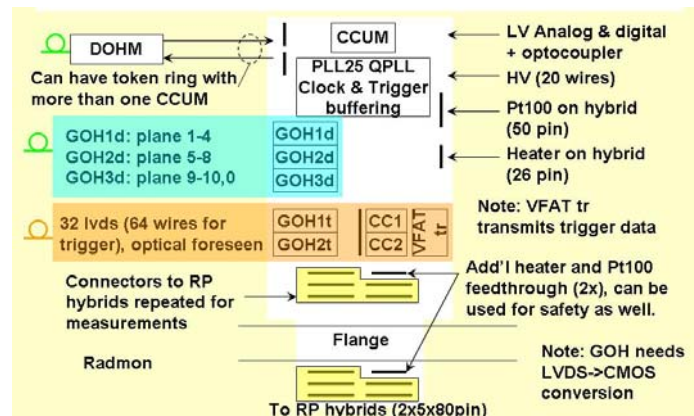


Fig. 5. The Roman Pot motherboard provides the interface to and from the outside world for the 10 detector hybrids of one Roman Pot.

Each Roman Pot is equipped with one **Roman Pot Motherboard** (see fig. 5) which performs the following functions:

1. It is glued through the flange closing the Roman Pot and provides the feedthrough from and to vacuum for the 10 Detector Hybrids, which are only connected to the outside world through the Motherboard.
2. It provides the feedthrough for all Roman Pot slow control items (temperature sensing and heaters, pressure sensors...). This is a much less bulky and costly way to realize the feedthroughs.
3. It is part of the electrical token-ring, carries a CCUM tec module for this purpose. This CCUM module converts the slow control signals to I2C and allows to control all items on the board and the hybrids which have an I2C interface. This interface is bidirectional – one can write and read registers. Reading registers is important for monitoring purposes (eg. DCU temperature measurement). In addition the CCUM provides a special clock/trigger signal which is converted to a trigger signal (including fast commands) and a clock signal. These are transmitted to the hybrids and converted to a separate clock and trigger signal there.
4. It provides the coincidence between the detector planes within one pot. For this purposes several CC chips are mounted. The resulting coincidence signals are electrically transferred (LVDS) to the counting room. There are 16 bits for U and 16 bits for V to be transferred, so 32 bits or 64 wires per pot. The cable between pots and station card will be as short as possible (~3 m). In addition to the coincidence signals a clock synchronized to the coincidence signals will be transmitted as well (1 bit, two additional wires).

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5. It carries the GOL Opto-Hybrids (GOH). These optohybrids carry each one GOL with matched laser transmitter. Each of the GOL can transmit the outputs of 16 VFATs. 3 GOHs (2.5 equipped) are needed to transmit the data of 40 VFAT chips. The readout data is therefore transferred directly from the Roman Pots to the counting Room. This means that the GOL Opto-Hybrids should come with at least 2 m pigtail length to reach the optical patch panel directly, otherwise some fanout with a local patch panel per group of three Roman Pots is needed to reach the fiber ribbon cable.
6. It receives the analog and digital power supply and the detector bias.
7. It provides the link for detector safety and radiation monitoring.

4 Roman Pot station overview

Fig. 6 gives an overview of the setup for one Roman Pot station which consists of two times 3 Roman Pots of 10 detector hybrids or planes each. The control, timing and trigger information for the 6 pots is handled by one TTC ring which follows the CMS tracker and ecal standard. A DOHM card receives and sends the optical information using two Digital Opto-Hybrids (DOH) and converts these optical signals from and to electrical signals for the token ring (CCU-ring), which starts from and returns to this card. The Roman Pot motherboard provides the interface between the detector and the outside world. Data, trigger generation, detector safety signals all leave from the motherboard directly to the counting room. The high voltage is supplied from the counting room. The low voltage is supplied from supplies placed in the caverns RR53/57 which convert 385 V DC into the appropriate voltages.

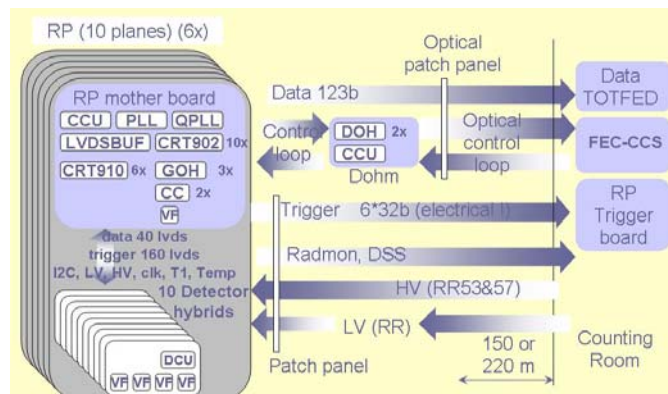


Fig.6. Overview of the electronics of one Roman Pot station

5 Roman Pot cabling

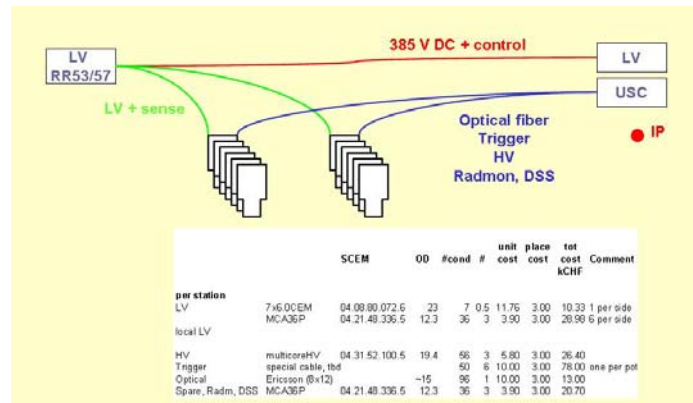


Fig.7. Cabling overview: the low voltage power supplies are located in the alcoves RR53/RR57. All the other connections are directly from the Roman Pot stations to the counting room

The low voltage power supplies will be located in the alcoves RR53/57, so power and control needs to be provided there and twisted screened cables for the LV and the sense wires will depart from there. The rest of the cables will leave directly from the Roman Pot stations to the counting room. An overview of the cables is shown in figure 7.

6 References

1. TOTEM TDR
2. Addendum to the TOTEM TDR
3. TOTEM general electronics specification
4. P. Aspell: VFAT digital part specification
5. J. Kaplon: Analog Front End
6. P. Chalmet, W. Snoeys: Coincidence Chip specification
7. P. Chalmet, W. Snoeys: LVDS repeater chip specification