

Specifications of the FEDCTOT05 front end (J. Kaplon)

All parameters given for nominal bias conditions unless otherwise noted.

Detector parameters

Coupling type to the amplifier; AC¹

Total capacitance seen by the FE input; 0 to 25pF, nominal 20pF

Total interstrip capacitance; maximum 75% of total detector capacitance²

Charge collection time; nominal 4ns, maximum 10ns

Input characteristic

Input signal polarity; positive or negative

Cross talk; <5% (via detector interstrip capacitance)

Maximum parasitic leakage current (in case of DC coupled detector); <25% preamplifier feedback current

Preamplifier Shaper characteristic

Architecture; single ended preamplifier and shaper stage AC coupled to the differential discriminator stage

Input transistor; NMOS 2000 μ m/0.5 μ m

Bias conditions of the front end stage:

- Power supply; 2.5V nominal, 2.25V minimum
- Input transistor bias; 450 μ A nominal, working range 300 μ A to 600 μ A
- Preamplifier feedback current; 800nA nominal, working range 500nA to 1.5 μ A
- Preamplifier buffer bias; 30 μ A nominal, working range 20 μ A to 40 μ A
- Shaper bias; 20 μ A, working range 20 to 40 μ A
- Shaper feedback bias; 20 μ A for positive input signals, 10 μ A for negative input signals, working range 5 μ A to 25 μ A
- Differential stage bias; 60 μ A nominal, working range 50 μ A to 80 μ A
- Comparator bias; 80 μ A nominal, working range 60 μ A to 100 μ A

Pulse Gain at discriminator input; 53mV/fC (simulated for maximum charge collection time)

Integral nonlinearity error:

- <1% for input charge 0 to 12fC
- <3% for input charge 0 to 16fC

Peaking time; 22.5ns (simulated for 3.5fC input charge and maximum charge collection time)

Power Supply Rejection Ratio at;

- 10Hz – 1kHz; >50dB
- 1kHz – 10kHz; >40dB
- 10kHz – 100kHz; >20dB
- 10MHz – 60MHz; >-3dB

Power consumption for nominal bias condition; 1.9mW/channel (250mW for whole front end)

¹ The front end can work with DC coupled detectors, however the analogue parameters are ensured for the detector leakage current less than 25% of preamplifier feedback bias current

² Maximum interstrip capacitance specified for the cross talk parameter

Noise performance for nominal bias condition³;

- <1000 e- rms for $C_{input} = 10\text{pF}$
- <1400 e- rms for $C_{input} = 20\text{pF}$

Maximum load of the analogue test outputs; <5pF

Comparator stage

Threshold setting equivalent to 1fC; 50mV

Threshold DAC range; $\pm 850\text{mV}$ equivalent to $\pm 11.6\text{fC}$

Threshold DAC step; 3.3mV (0.045fC)

Threshold spread (before trimming⁴); <4mV rms

Threshold Trim DAC range; 45mV (0.9fC)

Threshold Trim DAC step; 1.4mV (0.028fC)

Time walk (defined as maximum time variation in the crossing of the time stamp threshold over a signal range of 1.25 fC to 12 fC, with the comparator threshold set to 1fC); 12.5ns (simulated for maximum charge collection time)

Double pulse resolution; <75ns (for a 3.5fC signal followed by 3.5fC signal)

³ Assuming negligible contribution from detector leakage current

⁴ Data from the ABCDS/FE chip