Specifications of the FEDCTOT05 front end (J. Kaplon)

All parameters given for nominal bias conditions unless otherwise noted.

**Detector parameters**

Coupling type to the amplifier; AC\(^1\)

Total capacitance seen by the FE input; 0 to 25pF, nominal 20pF

Total interstrip capacitance; maximum 75% of total detector capacitance\(^2\)

Charge collection time; nominal 4ns, maximum 10ns

**Input characteristic**

Input signal polarity; positive or negative

Cross talk; <5% (via detector interstrip capacitance)

Maximum parasitic leakage current (in case of DC coupled detector); <25% preamplifier feedback current

**Preamplifier Shaper characteristic**

Architecture; single ended preamplifier and shaper stage AC coupled to the differential discriminator stage

Input transistor; NMOS 2000µm/0.5µm

Bias conditions of the front end stage:

- Power supply; 2.5V nominal, 2.25V minimum
- Input transistor bias; 450µA nominal, working range 300µA to 600µA
- Preamplifier feedback current; 800nA nominal, working range 500nA to 1.5µA
- Preamplifier buffer bias; 30µA nominal, working range 20µA to 40µA
- Shaper bias; 20µA, working range 20 to 40µA
- Shaper feedback bias; 20µA for positive input signals, 10µA for negative input signals, working range 5µA to 25µA
- Differential stage bias; 60µA nominal, working range 50µA to 80µA
- Comparator bias; 80µA nominal, working range 60µA to 100µA

Pulse Gain at discriminator input; 53mV/fC (simulated for maximum charge collection time)

Integral nonlinearity error:

- <1% for input charge 0 to 12fC
- <3% for input charge 0 to 16fC

Peaking time; 22.5ns (simulated for 3.5fC input charge and maximum charge collection time)

Power Supply Rejection Ratio at;

- 10Hz – 1kHz; >50dB
- 1kHz – 10kHz; >40dB
- 10kHz – 100kHz; >20dB
- 10MHz – 60MHz; >-3dB

Power consumption for nominal bias condition; 1.9mW/channel (250mW for whole front end)

---

\(^1\) The front end can work with DC coupled detectors, however the analogue parameters are ensured for the detector leakage current less than 25% of preamplifier feedback bias current

\(^2\) Maximum interstrip capacitance specified for the cross talk parameter
Noise performance for nominal bias condition:\n\begin{itemize}
\item $<1000 \text{ e- rms for } C_{\text{input}} = 10\text{pF}$
\item $<1400 \text{ e- rms for } C_{\text{input}} = 20\text{pF}$
\end{itemize}
Maximum load of the analogue test outputs; $<5\text{pF}$

**Comparator stage**

Threshold setting equivalent to $1\text{fC}$; $50\text{mV}$
Threshold DAC range: $\pm 850\text{mV}$ equivalent to $\pm 11.6\text{fC}$
Threshold DAC step; $3.3\text{mV}$ ($0.045\text{fC}$)
Threshold spread (before trimming$^4$); $<4\text{mV}$ rms
Threshold Trim DAC range; $45\text{mV}$ ($0.9\text{fC}$)
Threshold Trim DAC step; $1.4\text{mV}$ ($0.028\text{fC}$)

Time walk (defined as maximum time variation in the crossing of the time stamp threshold over a signal range of $1.25 \text{ fC}$ to $12 \text{ fC}$, with the comparator threshold set to $1\text{fC}$); $12.5\text{ns}$ (simulated for maximum charge collection time)

Double pulse resolution; $<75\text{ns}$ (for a $3.5\text{fC}$ signal followed by $3.5\text{fC}$ signal)

---

$^3$ Assuming negligible contribution from detector leakage current
$^4$ Data from the ABCDS/FE chip