

# CMS Ecal LVDS\_RX ASIC

Data Sheet V0.0 -> Preliminary Data Sheet 20/01/04

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## DESCRIPTION

The LVDS\_RX circuit is a eight channel differential line receiver especially designed for the CMS Ecal VFE electronic. It is designed to withstand high radiation doses (up to 10Mrad-Si and  $10^{14}$  N/cm<sup>2</sup>). The device supports data rates higher than 80Mb/s (40MHz).

The LVDS\_RX accepts differential input signal (typ 200mV) and translates them to CMOS output levels.

The input comparators have no hysteresis. The circuit operates from a single 2.5V supply although analog and digital supplies are available through separate pins.

## PROCESS

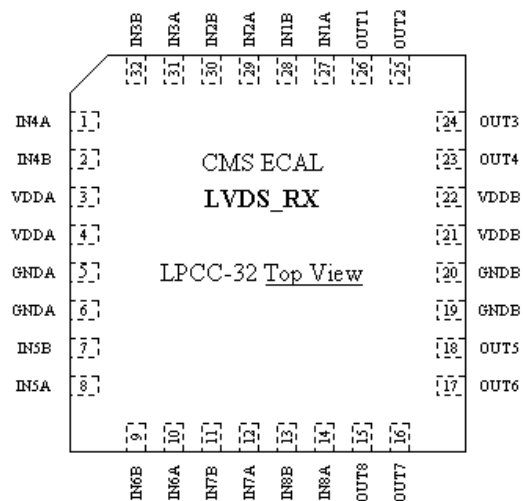
- 0.25μm CMOS (2.5V)

## FEATURES

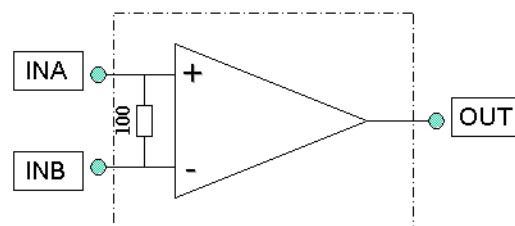
- 8 LVDS to CMOS line receivers
- Integrated 100Ω line termination
- Accept swing as small as 100mV
- Full ESD protections
- 32 pins LPCC Package (body 5x5 mm). (optional TQFP32)
- Operates from a single 2.5V Supply
- Typical Propagation Delay Time of 2 ns.
- Output Skew < 900ps
- Part-to-Part Skew < 1.4ns

- Open-Circuit Fail Safe mode and channel disabling capability are not implemented in this IC
- Chip size: 2mm\*2mm

## BONDING DIAGRAM



## LOGIC DIAGRAM

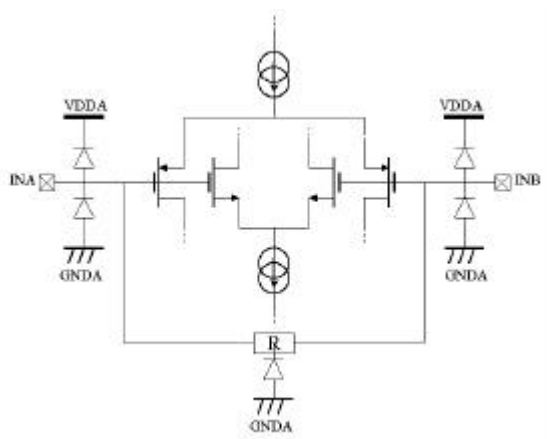


1/8 of CMS-ECAL LVDS\_RX Receiver

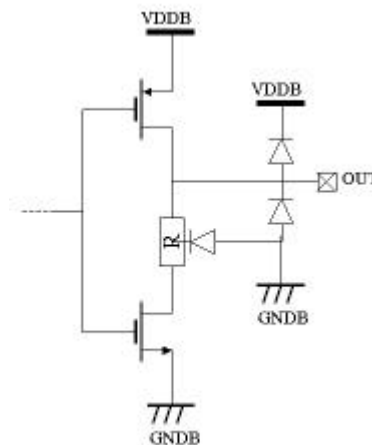
## FUNCTION TABLE

DIFFERENTIAL INPUT $V_{diff}=V(INA-INB)$	OUTPUT
$V_{diff}=100mV$	H
$-100mV < V_{diff} < 100mV$	Undefined
$V_{diff} = -100mV$	L

**Equivalent input schematic diagram**



**Equivalent output schematic diagram**



## DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{dd}$	Supply Voltage		2,3	2,5	2,7	V
$ V_{id} $	Differential Input Voltage	$ V_{INA}-V_{INB} $	100		800	mV
$V_{icm}$	Common Mode Input Voltage		$ V_{id} /2$		$V_{dd}- V_{id} /2$	V
$V_{in}$	Max Input Voltage Range	INA or INB	0		$V_{dd}$	V
$Z_{in}$	Differential Input impedance		85	100	115	$\Omega$
$C_{in}$	Input capacitance, A or B input to GND				5	pF
$V_{oh}$	High-level output voltage	$I_{oh} = -4 \text{ mA}$	1,7	2,3		V
$V_{ol}$	Low-level output voltage	$I_{ol} = 4 \text{ mA}$		0,25	0,5	V

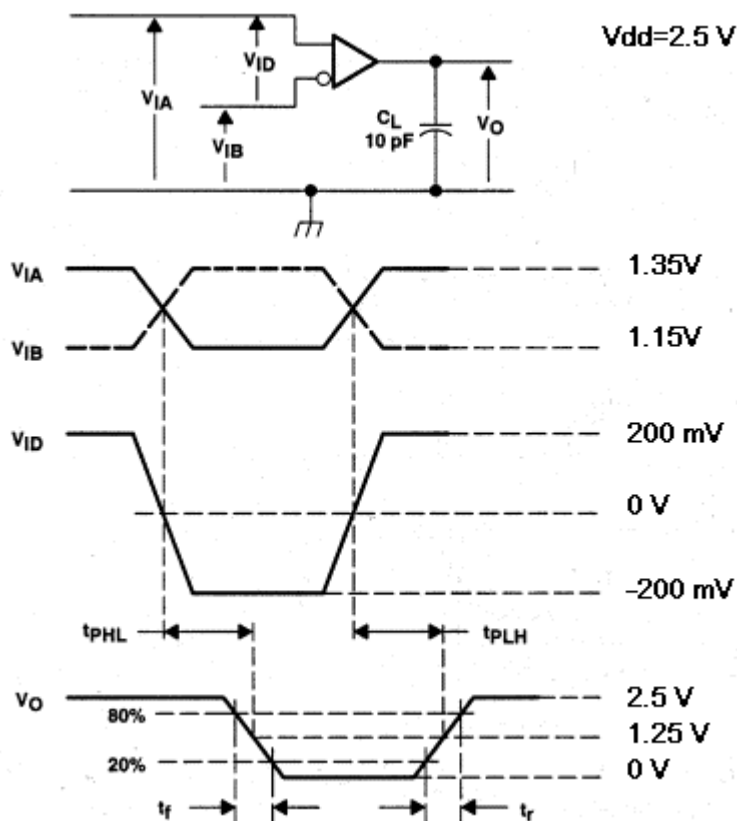
## AC CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tpHL	H to L propagation delay				2,9	ns
tpLH	L to H propagation delay				2,7	ns
tf	Output signal fall time				2,2	ns
tr	Output signal rise time				1,3	ns
tsk1	Channel to channel skew				900	ps
tsk2	Part to part skew	lot to lot			1,4	ns
fmax	Operating Frequency			40		MHz
Txs	Transmission Rate			80		Mb/s

## POWER REQUIREMENTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Icc	VDD DC Current Consumption				50	mA
Pd1	Power consumption @ 40MHz, Vdif=0,2V	Clload=10pF			160	mW
Pd2	Power consumption @ 80MHz, Vdif=0,2V	Clload=10pF			200	mW

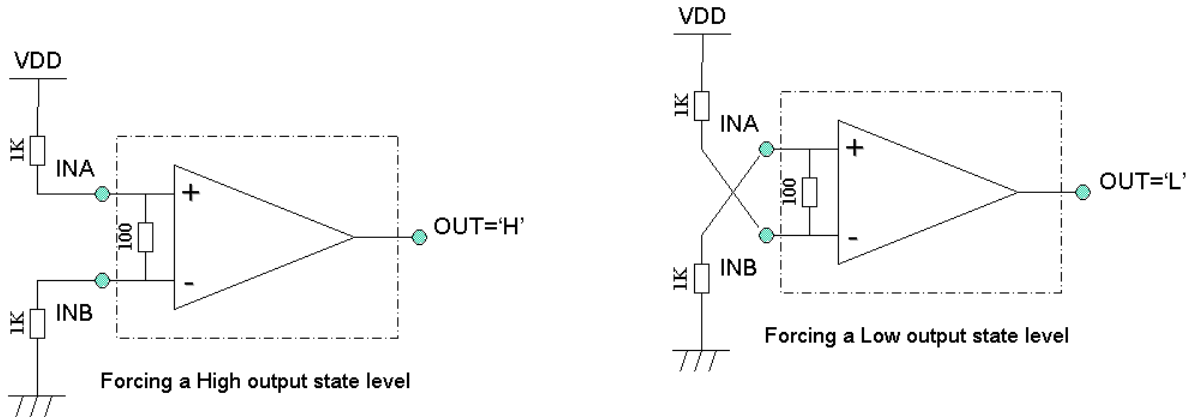
## PARAMETER MEASUREMENT INFORMATION



# APPLICATION INFORMATIONS

## UN-USED CHANNELS

Since there is no fail safe mode implemented in the LVDS\_RX receiver, unused channel inputs must be externally biased in order to guaranty a known level to the corresponding receiver output.



## TYPICAL APPLICATION

( Typical application schematic: ..in preparation)